DDR5 Client PMIC With I2C/I3C Interface

1 Description

The SY5888 is a power management IC (PMIC) for DDR5 SODIMM and UDIMM, and integrates three high efficiency Buck DC-DC converters, two LDOs, and flexible interface.

The device provides three channels buck outputs: SWA/SWB/SWC. SWA and SWB default are single phase and can be configured dual phase with current share operation.

VOUT_1.8V/VOUT_1.0V LDOs are intended to power supply SPD hub and Temp Sensor on DIMM. SY5888 is available FC-QFN28 3mmx4mm package, and is halogen and lead free, compliant with RoHS.

2 Applications

Small Outline(SODIMM)

Un-Buffered(UDIMM)DDR5-Based Dual in-line Memory Modules (DIMM)

3 Features

- VIN/VIN_Bulk Supply Range: 4.25V to 5.5V
- Three Buck Regulators:
  SWA (1 phase,default 1.1V,max 6A Valley)
  0.8V~2.2V，5mV/10mV step + offset
  SWB (1 phase,default 1.1V, max 6A Valley)
  0.8V~2.2V，5mV/10mV step + offset
  SWC (1 phase,default 1.8V, max 2A Valley)
  1.5V~2.135V，5mV step
- DCDC V_{OUT} Accuracy:±0.75% DC(FCCM)
  ±2.5% DC+AC
- F_{SW}: 0.75Mhz to 1.25Mhz with 250Khz step
- SWA/B Dual Phase Operation Configure
- Two Linear Regulators:
  - VOUT_1.8V: 1.7V to 2.0V with 0.1V step
  - VOUT_1.0V: 0.9V to 1.2V with 0.1V step
- Max to 1.0Mhz I2C Interface
- Support I2C 1.0V to 3.3VIO
- Max to 1.0VIO 12.5MHz I3C Interface
- Support Intel XMP3.0 OC Spec
- Support LDOs Power Reset
- Built-in MTP Non-Volatile Memory
- Support Secure&Programmable Mode
- Integrate ADC For Vol/Current/Power Consumption Monitor
- VIN_OVP/SWA/SWB/SWC OCP/UVP
- Over Temperature Protection
- PWR_GOOD&GSI_n to Indicate Status
- Compliant with JESD301-2 V1.0.3

4 Typical Application Circuit

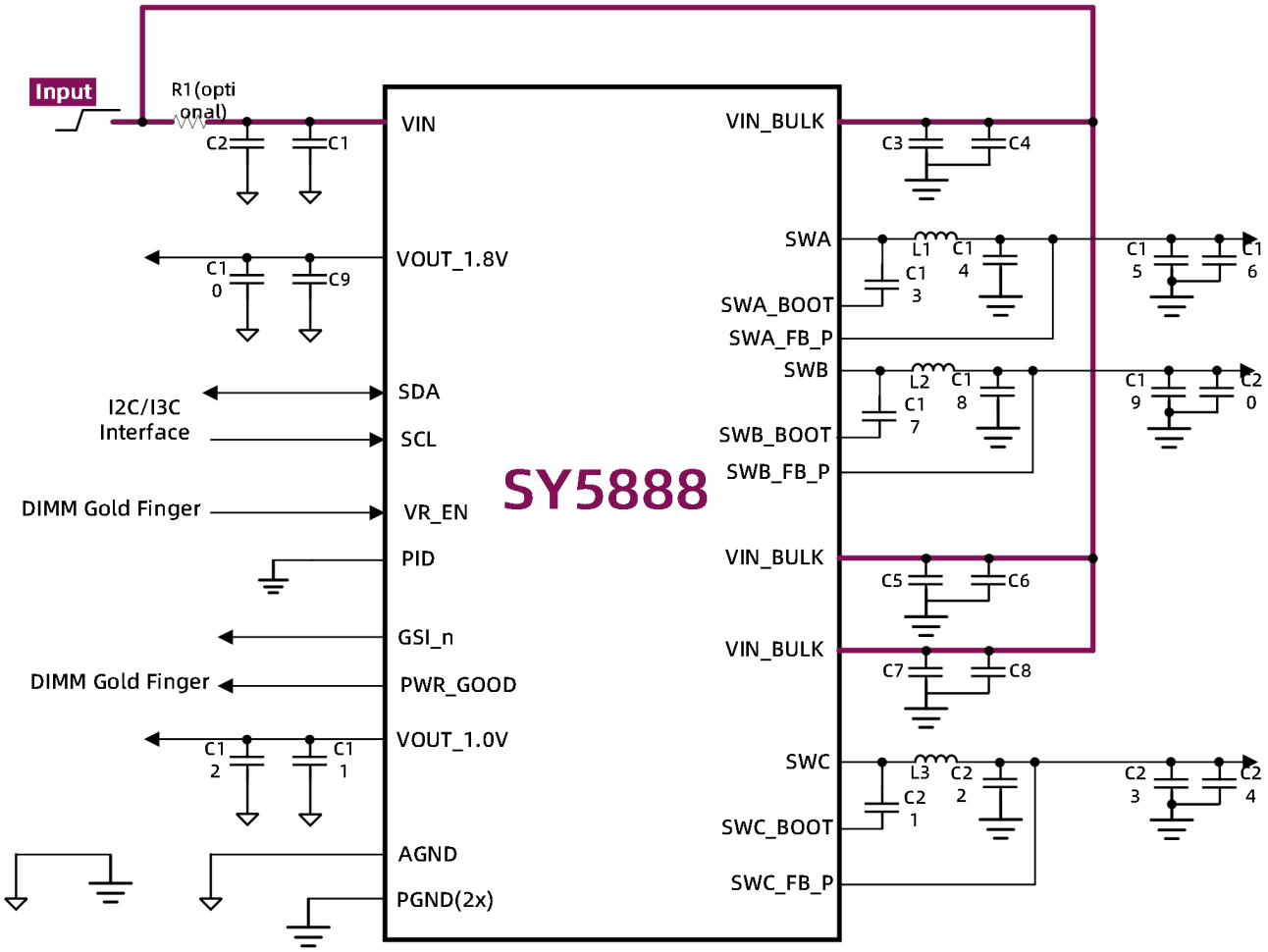

Figure 4- 1. Typical Application Circuit